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TITLE: SEMICONDUCTOR APPARATUS AND PROCESS OF PRODUCTION THEREOF

Hon. Commissioner for Patents,

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SIR;

CERTIFIED TRANSLATION

I, Mariko YOSHIDA, am an official translator of the Japanese language into the English language and I hereby certify that the attached comprises an accurate translation into English of Japanese Application No. H11-146942, filed on May 26, 1999.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Date Mariko YOSHIDA

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[TITLE OF THE INVENTION] Method Of Producing Semiconductor Apparatus

[CLAIMS]

[Claim 1]

A method of producing a semiconductor apparatus comprising the steps of:

forming bumps on a semiconductor wafer formed with a circuit pattern of a semiconductor chip so as to connect to the circuit pattern;

forming a resin film on a bumps forming surface of the semiconductor wafer so as to seal spaces between the bumps and to become a thickness forming a surface lower than a height of the bumps; and

cleaning the surfaces of the bumps projecting out from the surface of the resin film.

[Claim 2]

A method of producing a semiconductor apparatus as set forth in claim 1, wherein, in the step of cleaning the surface of the bumps, the surfaces of the bumps are activated in parallel.

[Claim 3]

A method of producing a semiconductor apparatus as set forth in claim 1, wherein, in the step of cleaning the surface of the bumps, the resin film components

deposited on the bumps are removed.

[Claim 4]

A method of producing a semiconductor apparatus as set forth in claim 1, wherein, in the step of cleaning the surface of the bumps, oxides on the bump surfaces are removed.

[Claim 5]

A method of producing a semiconductor apparatus as set forth in claim 1, wherein, in the step of cleaning the surface of the bumps, the resin film components are removed by irradiating a laser beam.

[Claim 6]

A method of producing a semiconductor apparatus as set forth in claim 1, wherein, in the step of cleaning the surface of the bumps, it is performed under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

[Claim 7]

A method of producing a semiconductor apparatus as set forth in claim 1, wherein, in the step of cleaning the surface of the bumps, it is performed while applying a gas jet to the bumps from a gas jet nozzle provided in the vicinity of the bumps to peel off a region in the vicinity of the bumps by a vacuum nozzle provided in the vicinity of the bumps.

[Claim 8]

A method of producing a semiconductor apparatus as set forth in claim 1, further comprising a step of forming eutectic solder layers on the bumps after the step of cleaning the surface of the bumps.

[Claim 9]

A method of producing a semiconductor apparatus as set forth in claim 8, wherein, in the step of forming the eutectic solder layers on the bumps, the eutectic solder layers are formed by a printing method, plating method, or transfer method.

[Claim 10]

A method of producing a semiconductor apparatus as set forth in claim 1, further comprising a step of cutting the semiconductor wafer into unit semiconductor chips after the step of cleaning the surface of the bumps.

[Claim 11]

A method of producing a semiconductor apparatus as set forth in claim 10, further comprising a step of mounting the semiconductor chip on a mounting board from the bump forming surface side so as to connect it at the bumps after cutting the semiconductor wafer into unit semiconductor chips.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a method of producing a semiconductor apparatus, particularly, a method of producing a semiconductor apparatus having a form of packaging reducing in size and higher in density.

[0002]

[Prior Art]

There are mounting demands for reducing the size, reducing the thickness, and reducing the weight of digital video cameras, digital cellular phones, notebook-type personal computers, and other portable electronic equipment. To respond the above, it is realized that recent VLSI or other semiconductor device is reduced in size of 70% for three years, and the improvement of the mounting density of the components on a mounting board has been researched and developed as the most important issue.

[0003]

Conventionally, as the form of packaging of semiconductor apparatuses, use has been made of DIP (Dual Inline Package) or PGA (Pin Grid Array) and other through hole mounted devices (THD) mounted to printed circuit boards by inserting leads through holes provided there and QFP (Quad Flat (L-Leaded) Package) or TCP (Tape Carrier Package) or other surface mounted devices (SMD)

mounted by soldering leads to the surfaces of the boards.

To further reduce sizes, attention has focused on the method of mounting a semiconductor chip with its pad opening surface facing the mounting board by a package called a chip size package (CSP, also called a FBGA (Fine-Pitch BGA)) for realizing further smaller sizes and higher densities to bring the package size extremely close to the size of the semiconductor chip (flip-chip mounting). Active research has been conducted up until now and numerous proposals have been made.

[0004]

A semiconductor apparatus mounting a CSP type semiconductor chip on a mounting board will be explained with reference to the drawings.

FIG. 8 is a cross-sectional view of the above semiconductor apparatus.

The surface of a semiconductor chip 10' on which electrode pads 11 comprised of Al etc. are formed is covered for example by a first surface protective film 12 comprised of a silicon nitride layer and a second surface protective film 13 comprised of a polyimide layer in a state leaving only the electrode pad 11 portions open. Further, a conductive film 14 comprised of a stacked films of chrome, copper, gold, etc. is formed at the apertures of the electrode pad 11 portions to be

connected to the electrode pads 11. The conductive film is sometimes called a BLM (Ball Limiting Metal) film.

Further, bumps 16b comprised of for example high melting point solder balls are formed connected to the conductive film (BLM film) 14.

A CSP type semiconductor chip 1 is constituted in this way.

[0005]

On the other hand, the mounting board 2 is a board 20 comprised of for example a glass epoxy-based material on the top of which are provided lands (electrodes) 21 formed at positions corresponding to the positions of formation of the bumps 16b of the semiconductor chip 1 to be mounted and comprised of copper etc. and a not shown printed circuit connected to the lands 21 and formed on the front surface or back surface or the two surfaces of the board 20. The surface of the board 20 other than the land 21 portions is covered by a solder resist 23.

[0006]

The above CSP type semiconductor chip 1 is mounted on the mounting board 2 with the bumps 16b aligned with the lands 21. The bumps 16b and lands 21 are mechanically and electrically connected by eutectic solder layers 19.

Further, the space between the CSP type semiconductor chip 1 and the mounting board 2 is sealed

by a sealing resin 3 comprised of an epoxy resin etc.

[0007]

In the above semiconductor apparatus, as the method of forming the bumps at predetermined positions, for example there is known the method of using electrolytic plating. In this case, there is the disadvantage that the thickness of the solder bumps formed is affected by the surface conditions of the layer of material forming the underlayer of the bumps or the slight variation in the electrical resistance and that the formation of uniform solder bumps of the same height in a semiconductor chip is extremely difficult.

[0008]

A method is being developed for formation of solder ball bumps with a uniform height using formation of a solder film by vacuum deposition and lift-off of the photoresist layer. This method will be explained below with reference to the drawings.

First, as shown in FIG. 9(a), electrode pads 11 comprised of an aluminum (Al) and copper (Cu) alloy etc. are formed by patterning on a semiconductor wafer 10 formed with circuit patterns of semiconductor chips by for example the sputtering method or etching etc. and a surface protective film 13 comprised of for example a silicon nitride layer or polyimide layer etc. is formed

on top of it covering the entire surface.

The electrode pad 11 portions of the surface protective layer 13 are opened, then for example a pattern is formed by the sputtering method so as to connect the conductive layer (BLM layer) 14 comprised of a stacked film of chrome, copper, and gold to the electrode pads 11.

[0009]

Then, as shown in FIG. 9(b), a resist film R2 having pattern apertures P is formed by patterning at the conductive film (BLM film) 14 forming areas by a photolithography step.

Then, as shown in FIG. 9(c), solder layers 16 are formed in the pattern apertures P of the resist film R2 by forming a solder layer over the entire surface by for example a vacuum evaporation method. At this time, solder layers 16a are formed over the resist film R2 as well.

[0010]

Then, as shown in FIG. 10(d), the solder layers 16a formed over the resist film R2 are simultaneously removed by removing the resist film R2 by lift-off. Due to this, it is possible to leave only the solder layers 16 formed in the pattern apertures P of the resist film R2.

Then, as shown in FIG. 10(e), heat treatment is performed to make the solder layers 16 melt. These are

cooled and solidified in a state forming spheres due to the surface tension so as to form solder ball bumps 16b.

[0011]

The thermal stress becomes a major disadvantage for the reliability of the joint by the bumps after flip-chip mounting due to the differences in the coefficients of heat expansion of the semiconductor chips and the mounting board (printed circuit board).

While the coefficient of heat expansion of silicon is 3.4 ppm/°C, the coefficient of heat expansion of the generally widely used glass epoxy-based mounting board is a large about 15 ppm/°C. When thermal stress is repeatedly applied to bump joints by the temperature difference caused by the on/off operation of a chip, cracks are caused in the joints and breakage or malfunctions are caused in some cases.

[0012]

To deal with the above disadvantage, the method is generally adopted of injecting a sealing resin between the semiconductor chips and mounting board and relieving the thermal stress applied to the weak strength bump joints by having the stress of heat expansion received by the sealing resin as a whole.

[0013]

In the above flip-chip mounting method of the

related art, however, since the semiconductor chips and the mounting board are secured by a sealing resin, when a defect occurs in a device chip, the only method was to discard the entire mounting board on which that semiconductor chip was mounted or apply a chemical or mechanical external force to forcibly tear off that semiconductor chip. Therefore, the work of replacing a defective component (rework) is difficult. This has become one factor behind the failure of flip-chip mounting from spreading widely.

[0014]

As a method for overcoming the above disadvantage, the method of reinforcing the bases of the bumps by coating epoxy-based resin to a device wafer formed the bumps at a wafer level and curing the resin has been developed.

[0015]

The above method will be explained with reference to the drawings.

FIG. 11 is a cross-sectional view of a semiconductor apparatus formed by the above method.

The surface of a semiconductor chip 10′ on which electrode pads 11 comprised of Al etc. are formed is covered for example by a surface protective film 13 comprised of a silicon nitride layer or a polyimide layer

in a state leaving only the electrode pad 11 portions open. Further, the conductive film (BLM film) 14 comprised of a stacked films of chrome, copper, gold, etc. is formed at the apertures to be connected to the electrode pads 11. Further, an upper surface protective film 15 for example comprised of polyimide is formed on the conductive film (BLM) film 14 with a bumps formation region opening.

Further, bumps 16b comprised of for example high melting point solder balls are formed connected to the conductive film (BLM film) 14. Here, to avoid a contact with adjoining bumps, the bumps 16 are formed at different positions from positions of formation of electrode pads 11 if necessary, and the conductive film (BLM film) 14 is formed by patterning to correspond to the above.

The surface of the semiconductor chip 10' in spaces between the bumps 16b (actually, the upper surface protective film 15 etc.) is sealed by a resin film 17 of epoxy-based resin.

A CSP type semiconductor chip 1 is constituted in this way.

[0016]

On the other hand, the mounting board 2 is a board 20 comprised of for example a glass epoxy-based material

on the top of which are provided lands (electrodes) 21 formed at positions corresponding to the positions of formation of the bumps 16b of the semiconductor chip 1 to be mounted and comprised of copper etc. and a not shown printed circuit connected to the lands 21 and formed on the front surface or back surface or the two surfaces of the board 20. The surface of the board 20 other than the land 21 portions is covered by a solder resist 23.

[0017]

The above CSP type semiconductor chip 1 is mounted on the mounting board 2 with the bumps 16b aligned with the lands 21. The bumps 16b and the lands 21 are mechanically and electrically connected by eutectic solder layers 19.

[0018]

The above method of producing the semiconductor apparatus will be explained below with reference to the drawings.

First, as shown in FIG. 12(a), electrode pads 11 comprised of an aluminum (Al) and copper (Cu) alloy etc. are formed by patterning on a semiconductor wafer 10 formed with circuit patterns of semiconductor chips by for example the sputtering method or etching etc. and a surface protective film 13 comprised of for example a silicon nitride layer or polyimide layer etc. is formed

on top of it covering the entire surface. The electrode pad 11 portions of the surface protective layer 13 are opened.

[0019]

Then, as shown in FIG. 12(b), a resist film R1 is formed with pattern by photolithography step to open a conductive film forming region of connecting the electrode pads 11 to the bumps 16b to be formed by the latter step, then a conductive layer (BLM layer) 14 is formed over the resist film by for example sputtering method by depositing a stacked film of chrome, copper, and gold so as to connect the electrode pads 11 in pattern apertures of the resist film R1. At this time, the conductive film 14a is formed over the resist film R1 as well.

[0020]

Then, as shown in FIG. 12(c), the conductive layers 14a formed over the resist film R1 are simultaneously removed by removing the resist film R1 by lift-off. Due to this, it is possible to leave only the conductive layers (BLM film) 14 formed in the pattern apertures of the resist film R1.

[0021]

Then, as shown in FIG. 13(d), the upper surface protective film 15 comprised of for example a polyimide

layer is formed over the conductive film (BLM film) 14 and opened to form bumps forming areas.

[0022]

Then, as shown in FIG. 13(e), a resist film R2 having pattern apertures is formed by patterning at the bump forming areas by a photolithography step.

Then, solder layers 16 are formed in the pattern apertures of the resist film R2 by forming a solder layer over the entire surface by for example a vacuum evaporation method. At this time, solder layers 16a are formed over the resist film R2 as well.

[0023]

Then, as shown in FIG. 13(f), the solder layers 16a formed over the resist film R2 are simultaneously removed by removing the resist film R2 by lift-off. Due to this, it is possible to leave only the solder layers 16 formed in the pattern apertures of the resist film R2.

[0024]

Then, as shown in FIG. 14(g), heat treatment is performed to make the solder layers 16 melt. These are cooled and solidified in a state forming spheres due to the surface tension to form solder ball bumps 16b.

[0025]

Then, as shown in FIG. 14(h), a resin film 17 is formed at the bumps 16b forming surface of the

semiconductor wafer 10 while sealing the spaces between the bumps 16b.

[0026]

Then, as shown in FIG. 15(i), eutectic solder layers 18 are formed by the printing method, plating method, or transfer method connected to the bumps 16a.

Then, the semiconductor wafer 10 is cut along the cutting positions D of the semiconductor wafer 10 by a dicing step to divide it into individual CSP type semiconductor chips 1.

[0027]

Then, as shown in FIG. 15(j), the CSP type semiconductor chip 1 is mounted on a mounting board 2 from the bump 16b forming surface.

The mounting board 2 is a board 20 comprised of for example a glass epoxy based material on the top of which are provided lands (electrodes) 21 formed at positions corresponding to the positions of formation of the solder bumps 16b of the semiconductor chip 1 to be mounted and comprised of copper etc. and a not shown printed circuit connected to the lands 21 and formed on the front surface or back surface or the two surfaces of the board 20. A precoated solder layer 22 is formed on the lands 21. Further, the surface of the board 20 other than the land 21 portions is covered by a solder resist 23.

The above CSP type semiconductor chip 1 is mounted on the above mounting board 2 with the bumps 16b aligned with the lands 21. By making the eutectic solder layer 18 or precoated solder layer 22 reflow, eutectic solder layers 19 are formed at the joint positions of the bumps 16b and lands 21, and the CSP type semiconductor chip 1 and mounting board 2 are mechanically and electrically connected to produce the semiconductor device shown in FIG. 11.

[0028]

The above semiconductor apparatus is reinforced with the bases of the bumps by the resin film sealing the spaces between the bumps. Even if the area between the semiconductor chips and the mounting board is not completely sealed by the resin, it is possible to increase the resistance to heat expansion stress and improve the connection reliability, the removal of a CSP type semiconductor chip from the mounting board is easy, and the work of replacement of defective components (rework) is simple.

[0029]

[Problem to be Solved by the Invention]

However, in the above method of producing the semiconductor apparatus, as shown in FIG. 14(h), when a resin film 17 is formed at the bumps 16a forming surface

of the semiconductor wafer 10 while sealing the spaces between the bumps 16a, resin coating components or oxides of the solder and other insulating impurities 17a are formed on the surfaces of the bumps 16b depending on the process conditions of the resin coating step. In the drawings, for convenience, a thickness greater than the actual insulating impurities is shown.

As described above, the formed insulating impurities 17a are remained at bumps joint interfaces after mounting the mounting board 2 as shown in FIG. 11, so a rise in the electrical resistance and decline in the joint strength etc. occur or the connection reliability in the bumps joint is deviated.

[0030]

An object of the present invention is to provide a method of producing a semiconductor apparatus which can suppress a rise in the electrical resistance and a decline in the joint strength at the bump joint interfaces and improve the connection reliability when using the method of reinforcing the bases of the bumps by a resin film of sealing the space between the bumps.

[0031]

[Means for Solving the Problem]

A method of producing a semiconductor apparatus has the steps of: forming bumps on a semiconductor wafer

formed with a circuit pattern of a semiconductor chip so as to connect to the circuit pattern; forming a resin film on a bumps forming surface of the semiconductor wafer so as to seal spaces between the bumps and to become a thickness forming a surface lower than a height of the bumps; and cleaning the surfaces of the bumps projecting out from the surface of the resin film.

[0032]

In the method of producing a semiconductor apparatus of the present invention, preferably, in the step of cleaning the surface of the bumps, the surfaces of the bumps are activated in parallel.

[0033]

In the method of producing a semiconductor apparatus on the present invention, preferably, in the step of cleaning the surface of the bumps, the resin film components or oxides deposited on the bumps are removed to clean the surface of the bumps.

[0034]

In the method of producing a semiconductor apparatus of the present invention, preferably, in the step of cleaning the surface of the bumps, the resin film components are removed by irradiating a laser beam under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere while applying a gas jet to

the bumps from a gas jet nozzle provided in the vicinity of the bumps to peel off a region in the vicinity of the bumps by a vacuum nozzle provided in the vicinity of the bumps.

[0035]

The method of producing a semiconductor apparatus of the present invention preferably further has a step of forming eutectic solder layers on the bumps by a printing method, plating method, or transfer method after the step of cleaning the surface of the bumps.

[0036]

The method of producing a semiconductor apparatus of the present invention further has a step of cutting the semiconductor wafer into unit semiconductor chips after the step of cleaning the surface of the bumps, and mounting the semiconductor chip on a mounting board from the bump forming surface side so as to connect it at the bumps.

[0037]

In the method of producing a semiconductor apparatus of the present invention, the bumps is formed on the semiconductor wafer formed with the circuit pattern of the semiconductor chip so as to connect to the circuit pattern, the resin film is formed on the bumps forming surface of the semiconductor wafer while sealing

the space between the bumps with a thickness to become a thickness forming a surface lower than the height of the bumps. Further, by irradiating a laser beam, extremely sharp heat expansion is caused at the surface portions of the bumps, then the sealing resin components are peeled off and a gas jet is applied to remove them or the energy of the laser beam may be used to reduce the surface portions of the bumps and remove the natural oxides to clean and activate the surfaces of the bumps.

[0038]

Further, by cleaning the surfaces of the bumps under a reducing atmosphere, an inert gas atmosphere, or a reducing gas atmosphere, it is possible to suppress the progress of natural oxidation after the cleaning.

[0039]

According to the method of producing a semiconductor apparatus of the present invention, by using the method of reinforcing the bases of the bumps by a resin film of sealing the space between the bumps, the resin film components or oxides are removed from the surface of the bumps projecting out from the resin film surface to clean and activate the surface of the bumps, and then it is mounted on the mounting board. Therefore, a rise in the electrical resistance and a decline in the joint strength at the bump joint interfaces can be

suppressed and the connection reliability is improved.

[0040]

By supplying the eutectic solder layer after cleaning the surface of the bumps, the height of the bumps is made high to improve the thermal stress resistance and improve a wettability of the solder in mounting the mounting board, whereby the connecting reliability can be further improved.

[0041]

[Embodiment of the Invention]

Below, embodiments of a method of producing a semiconductor apparatus according to the present invention will be explained with reference to the drawings.

[0042]

FIG. 1 is a cross-sectional view of a semiconductor apparatus produced by the method of producing a semiconductor apparatus according to the present embodiment.

A surface of a semiconductor chip 10′ for forming electrode pads 11 comprised of aluminum etc. is for example covered by a surface protective film 13 comprised of for example a silicon nitride layer or polyimide layer, then electrode pads 11 portions are opened. A conductive film 14 comprised of a stacked film of chrome, copper,

and gold etc. is formed at apertures connected to the electrode pads 11. The conductive film is sometimes called a BLM (Ball Limiting Metal) film. Further, an upper surface protective film 15 comprised of for example a polyimide is formed on the conductive film (BLM film) 14 and bump forming areas are opened.

In the above bump forming regions, bumps 16b comprised of for example high melting point solder balls are formed connected to the conductive film (BLM film) 14. Here, to avoid contact with the adjoining bumps etc., the positions of formation of the bumps 16b are shifted to the positions of formation of the electrode pads 11 if necessary and the conductive film (BLM film) 14 is formed by patterning so as to correspond to this.

The surface of the semiconductor chip 10' (in actuality, the upper surface protective film 15 etc.) at the spaces between the bumps 16b is sealed by a resin film 17 comprised of an epoxy resin etc.

A CSP type semiconductor chip 1 is constituted in this way.

[0043]

On the other hand, the mounting board 2 is a board 20 comprised of for example a glass epoxy based material on the top of which are provided lands (electrodes) 21 formed at positions corresponding to the positions of

formation of the solder bumps 16b of the semiconductor chip 1 to be mounted and comprised of copper etc. and a not shown printed circuit connected to the lands 21 and formed on the front surface or back surface or the two surfaces of the board 20. The surface of the board 20 other than the land 21 portions is covered by a solder resist 23.

[0044]

The above CSP type semiconductor chip 1 is mounted on a mounting board 2 with the bumps 16b aligned with the lands 21. The bumps 16b and lands 21 are mechanically and electrically connected by eutectic solder layers 19.

[0045]

The method of producing the above semiconductor apparatus will be explained with reference to the drawings.

First, as shown in FIG. 2(a), the electrode pads 11 comprised of an aluminum and copper alloy etc. are formed by patterning on a semiconductor wafer 10 formed with circuit patterns of semiconductor chips by for example the sputtering method or etching etc., a surface protective film 13 comprised of for example a silicon nitride layer or polyimide layer etc. is formed on top of it covering the entire surface, and electrode pads 11 portions of the surface protective layer 13 are opened.

[0046]

Next, as shown in FIG. 2(b), a resist film R1 in which regions for forming a conductive film connecting the electrode pads 11 and bumps formed in a later step are opened are formed by patterning by a photolithography step and a stacked film of chrome, copper, and gold is deposited on the entire surface by for example the sputtering method to form a conductive film (BLM film) 14 so as to connect the electrode pads 11 in the pattern apertures of the resist film R1. At this time, a conductive film 14a is formed on top of the resist film R1.

[0047]

Then, as shown in FIG. 2(c), the resist film R1 is removed by lift-off to simultaneously remove the conductive film 14a formed on the resist film R1. Due to this, it is possible to leave only the conductive film (BLM film) 14 formed in the pattern apertures of the resist film R1.

[0048]

Then, as shown in FIG. 3(d), an upper surface protective film 15 comprised of for example a polyimide layer etc. is formed on the conductive film (BLM film) 14 covering the entire surface and bump forming regions of the upper surface protective film 15.

[0049]

Then, as shown in FIG. 3(e), a resist film R2 having pattern apertures is formed by patterning at the bump forming regions by a photolithography step.

Then, a solder layer is formed over the entire surface by for example a vacuum evaporation method to form solder layers 16 in the pattern apertures of the resist film R2. At this time, solder layers 16a are formed over the resist film R2 as well.

[0050]

Then, as shown in FIG. 3(f), the solder layers 16a formed over the resist film R2 are simultaneously removed by removing the resist film R2 by lift-off. As a result, it is possible to leave only the solder layers 16 formed in the pattern openings of the resist film R2.

[0051]

Then, as shown in FIG. 4(g), heat treatment is performed to make the solder layers 16 melt. These are cooled and solidified in a state forming spheres due to the surface tension so as to form solder ball bumps 16b comprised of high melting point solder balls.

[0052]

Then, as shown in FIG. 4(h), for example, an epoxy-based resin is coated at the semiconductor wafer level, then the resin is treated to cure, a resin film 17 is

formed at the bumps 16a forming surface of the semiconductor wafer 10 at a thickness forming a surface lower than the height of the bumps 16b while sealing the spaces between the bumps 16b.

At this time, resin coating components or oxides of the solder and other insulating impurities 17a are formed on the surfaces of the bumps 16b depending on the process conditions of the resin coating step. In the drawings, for convenience, a thickness greater than the actual insulating impurities is shown.

[0053]

Then, as shown in FIG. 4(i), excimer leaser beam L is irradiated on the bumps 16a forming surface of the semiconductor wafer 10 to remove the resin coating components or oxides of the solder and other insulating impurities 17a from the surfaces of the bumps 16b to thereby clean the surfaces of the bumps 16b projecting out from the surface of the resin film 17.

[0054]

Here, the laser beam may be irradiated from a laser beam irradiation device such as shown in the schematic view of FIG. 6 for example.

The laser beam irradiation device is provided with a wafer stage 30, a not shown light source for irradiating an excimer laser beam L, a gas ejection

nozzle 33 for ejecting a gas 34, and a suction nozzle 35.

In the laser beam irradiation device, the semiconductor wafer 31 for processing is placed on and secured to the wafer stage 30 with the bump forming surface facing upward and a KrF excimer laser beam L with, for example, a wavelength of 248 nm, an energy density of 400 mJ/cm^2, and a pulse oscillation of 30 Hz is irradiated on the bump forming surface of the semiconductor wafer to sweep it at a speed of 50 mm/sec.

At this time, the nitrogen gas or other gas 34 is ejected from the gas ejection nozzle 33 provided at the laser beam irradiation device to the bump forming surface at a flow rate of 20 l/sec to peel off the sealing resin components and other insulating impurities 17a which are then sucked away by the suction nozzle 35.

Note that, the movement of the wafer stage 30 and laser pulses are synchronized and a laser beam irradiated at a constant overlap. The amount of irradiation of the laser beam is controlled to be uniform in the plane of the semiconductor wafer.

[0055]

Due to the above irradiation of a laser beam, extremely sharp heat expansion is caused at the surface portions of the bumps 16b, the sealing resin components deposited on the surfaces of the bumps 16b are peeled off,

and a gas jet is applied to remove them so as to clean the surfaces of the bumps. Further, the energy of the laser beam may be used to reduce the surface portions of the bumps and remove the natural oxides and activate the surfaces of the bumps.

[0056]

Further, the laser beam may be irradiated by a laser beam irradiation device such as shown in the schematic view of FIG. 7 for example.

The laser beam irradiation device is provided with a wafer cassette 37 in which untreated wafers 31 are housed, a reaction treatment chamber 36, and a load-lock chamber 39 in which treated wafers 31 are housed. The wafer cassette 37 and reaction treatment chamber 36 and the reaction treatment chamber 36 and load-lock chamber 39 are connected by gate valves 38.

In the reaction treatment chamber 36, the laser beam irradiation device is provided with a wafer stage 30, a not shown light source for irradiating the excimer laser beam L, a gas ejection nozzle 33 for ejecting a gas 34, and a suction nozzle 35.

Further, the reaction treatment chamber 36 is provided with a gas exhaust port 41 connecting the gas introduction port 40 to a not shown suction pump. The inside of the reaction treatment chamber 36 can be made a

reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

[0057]

In the above laser beam irradiation device, the air is exhausted from the gas exhaust port 41 to reduce the pressure, a nitrogen gas is introduced from the gas introduction port 40, and a not shown wafer operating mechanism is used to take out a semiconductor wafer to be treated from the wafer cassette 37 in the reaction treatment chamber 36 controlled to a 1 Torr nitrogen atmosphere and to place and secure the bump forming surface on the wafer stage 30 facing upward.

A KrF excimer laser beam L with, for example, a wavelength of 248 nm, an energy density of 400 mJ/cm^2, and a pulse oscillation of 30 Hz is irradiated on the bump forming surface of the semiconductor wafer to sweep it at a speed of 50 mm/sec.

At this time, the nitrogen gas or other gas 34 is ejected from the gas ejection nozzle 33 provided at the laser beam irradiation device to the bump forming surface at a flow rate of 20 l/sec to peel off the sealing resin components and other insulating impurities 17a which are then sucked away by the suction nozzle 35.

The treated semiconductor wafer 31 is housed in the load-lock chamber 39 by a not shown wafer operating

mechanism.

Note that, the movement of the wafer stage 30 and laser pulses are synchronized and a laser beam irradiated at a constant overlap. The amount of irradiation of the laser beam is controlled to be uniform in the plane of the semiconductor wafer.

[0058]

Due to the above irradiation of a laser beam, the sealing resin components deposited on the surfaces of the bumps 16b are peeled off and a gas jet is applied to remove them so as to clean the surfaces of the bumps. Further, it is possible to remove the natural oxides on the surfaces of the bumps and activate the surfaces of the bumps.

Further, by performing the above treatment in a reduced pressure atmosphere, inert gas atmosphere, or reducing gas atmosphere, the oxygen is removed from the reaction treatment chamber 36. The chamber becomes a high temperature by the cleaning by irradiation of a laser beam and the progress of natural oxidation of the activated surfaces of the bumps can be suppressed.

[0059]

Next, as shown in FIG. 5(j), a eutectic solder layer 18 is formed connected to the bumps 16a by the printing method, plating method, or transfer method. By

forming the eutectic solder layer 18, the height of the bumps is made high to improve the thermal stress resistance and the wettability of the solder in mounting on the mounting board can be improved. As a result, the connecting reliability can be further improved.

Then the semiconductor wafer 10 is cut along the cutting positions D of the semiconductor wafer 10 by a dicing step to divide it into individual CSP type semiconductor chips 1.

[0060]

Further, as shown in FIG. 5(k), a CSP type semiconductor chip 1 is mounted on the mounting board 2 from the bump 16b forming surface.

The mounting board 2 is a board 20 comprised of, for example, a glass epoxy based material on the top of which are provided lands (electrodes) 21 formed at positions corresponding to the positions of formation of the solder bumps 16b of the semiconductor chip 1 to be mounted and comprised of copper etc. and a not shown printed circuit connected to the lands 21 and formed on the front surface or back surface or the two surfaces of the board 20, a precoated solder layer 22 comprised of a eutectic solder formed on the lands 21, further the surface of the board 20 other than the land 21 portions being covered by a solder resist 23.

The above CSP type semiconductor chip 1 is mounted on the above mounting board 2 with the bumps 16b aligned with the lands 21. Heat treatment of, for example, 200 to 250°C is used to make the eutectic solder layer 18 or precoated solder layer 22 reflow without the bumps 16b melting, eutectic solder layers 19 are formed at the joint positions of the bumps 16b and lands 21, and the CSP type semiconductor chip 1 and mounting board 2 are mechanically and electrically connected to produce the semiconductor device shown in FIG. 1.

[0061]

In the semiconductor apparatus explained above, the bases of the bumps are reinforced by the resin film sealing the spaces between the bumps. Even if the area between the semiconductor chips and the mounting board is not completely sealed by the resin, it is possible to increase the resistance to heat expansion stress and improve the connection reliability, the removal of a CSP type semiconductor chip from the mounting board is easy, and the work of replacement of defective components (rework) is simple.

[0062]

Further, according to the method of producing a semiconductor apparatus of the present embodiment, irradiation by a laser beam etc. is used to cause

extremely sharp heat expansion at the surface portions of the bumps to peel off the sealing resin components which are then removed by a gas jet or the energy of the laser beam is used to reduce the surface portions of the bumps and remove the natural oxides so as to clean and activate the surfaces of the bumps before mounting, so a rise in the electrical resistance and a decline in the joint strength at the bump joint interfaces are suppressed and the connection reliability can be improved.

[0063]

Further, as the semiconductor apparatus produced by the present invention, any of a MOS transistor type semiconductor apparatus, bipolar type semiconductor apparatus, BiCMOS type semiconductor apparatus, semiconductor apparatus carrying logics and memories, and other semiconductor apparatuses may be applied.

[0064]

The method of producing a semiconductor apparatus of the present invention is not limited to the above embodiment.

For example, the configuration of the laser beam treatment device, conditions of the processes, structure of the wafer, etc. are not limited to the details explained in the above embodiments.

Further, the bumps may be formed on the wafer by

use of transfer of the solder balls and other various methods.

In addition, various changes may be made within the scope of the gist of the present invention.

[0065]

[Effect of the Invention]

As explained above, according to the method of producing the semiconductor apparatus of the present invention, it is possible to suppress an increase of the electric resistance and a reduction of the jointing strength in the bumps joint interface and improve the connection reliability when reinforcing the bases of the bumps by the resin film sealing the spaces between the bumps.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1] FIG. 1 is a cross-sectional view of a semiconductor apparatus according to an embodiment;

[FIG. 2] FIG. 2 is a cross-sectional view showing steps of a method of producing the semiconductor apparatus according to the embodiment, wherein (a) shows up to the step of opening electrode pads, (b) shows up to the step of forming a conductive layer (BLM film), and (c) shows up to the step of removing the conductive layer on a resist film by lift-off.

[FIG. 3] FIG. 3 shows the steps after FIG. 2,

wherein (d) shows up to the step of forming the surface protective film, (e) shows up to the step of depositing the solder layer, and (f) shows up to the step of removing the solder layer on the resist film by lift-off.

[FIG. 4] FIG. 4 shows the steps after FIG. 3, wherein (g) shows up to the step of forming the solder ball bumps by reflow, (h) shows up to the step of forming the resin coating, and (i) shows up to the step of cleaning the surfaces of the bumps.

[FIG. 5] FIG. 5 shows the steps after FIG. 4, wherein (j) shows up to the step of supplying the eutectic solder layers and (k) shows up to the step of mounting on the mounting board.

[FIG. 6] FIG. 6 is a schematic view of an excimer laser beam irradiation device according to the present embodiment.

[FIG. 7] FIG. 7 is a schematic view of an excimer laser beam irradiation device according to the present embodiment;

[FIG. 8] FIG. 8 is a cross-sectional view of a semiconductor apparatus according to a first conventional example.

[FIG. 9] FIG. 9 is a cross-sectional view of steps of a method of producing a semiconductor apparatus according to the first conventional example, wherein (a)

shows up to the step of forming a conductive film (BLM film), (b) shows up to the step of forming a resist film, and (c) shows up to the step of depositing the solder layer.

[FIG. 10] FIG. 10 shows the steps after FIG. 9, wherein (d) shows up to the step of removing the solder layer on a resist film by lift-off and (e) shows up to the step of forming solder ball bumps by reflow.

[FIG. 11] FIG. 11 is a cross-sectional view of a semiconductor apparatus according to a second conventional example.

[FIG. 12] FIG. 12 is a cross-sectional view of steps of a method of producing a semiconductor apparatus according to the second conventional example, wherein (a) shows up to the step of opening electrode pads, (b) shows up to the step of forming conductive film (BLM film), and (c) shows up to the step of removing the conductive film on the resist film by lift-off.

[FIG. 13] FIG. 13 shows the steps after FIG. 12, wherein (d) shows up to the step of forming a surface protective film, (e) shows up to the step of depositing the solder layer, and (f) shows up to the step of removing the solder layer on the resist layer by lift-off.

[FIG. 14] FIG. 14 shows the steps after FIG. 13, wherein (g) shows up to the step of forming solder ball

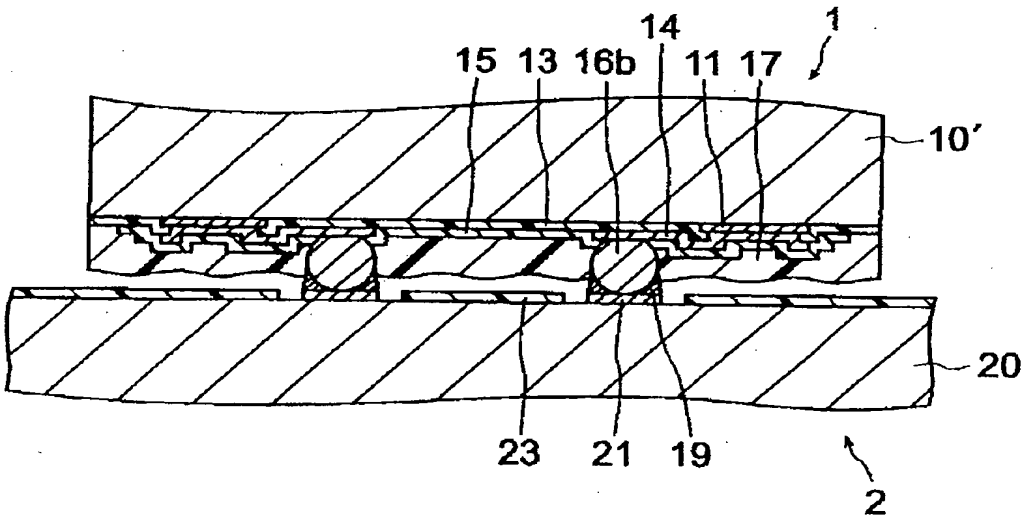
bumps by reflowing and (h) shows up to the step of forming a resin film.

[FIG. 15] FIG. 15 shows the steps after FIG. 14, wherein (i) shows up to the step of supplying an eutectic solder layer and (j) shows up to the step of mounting on the mounting board.

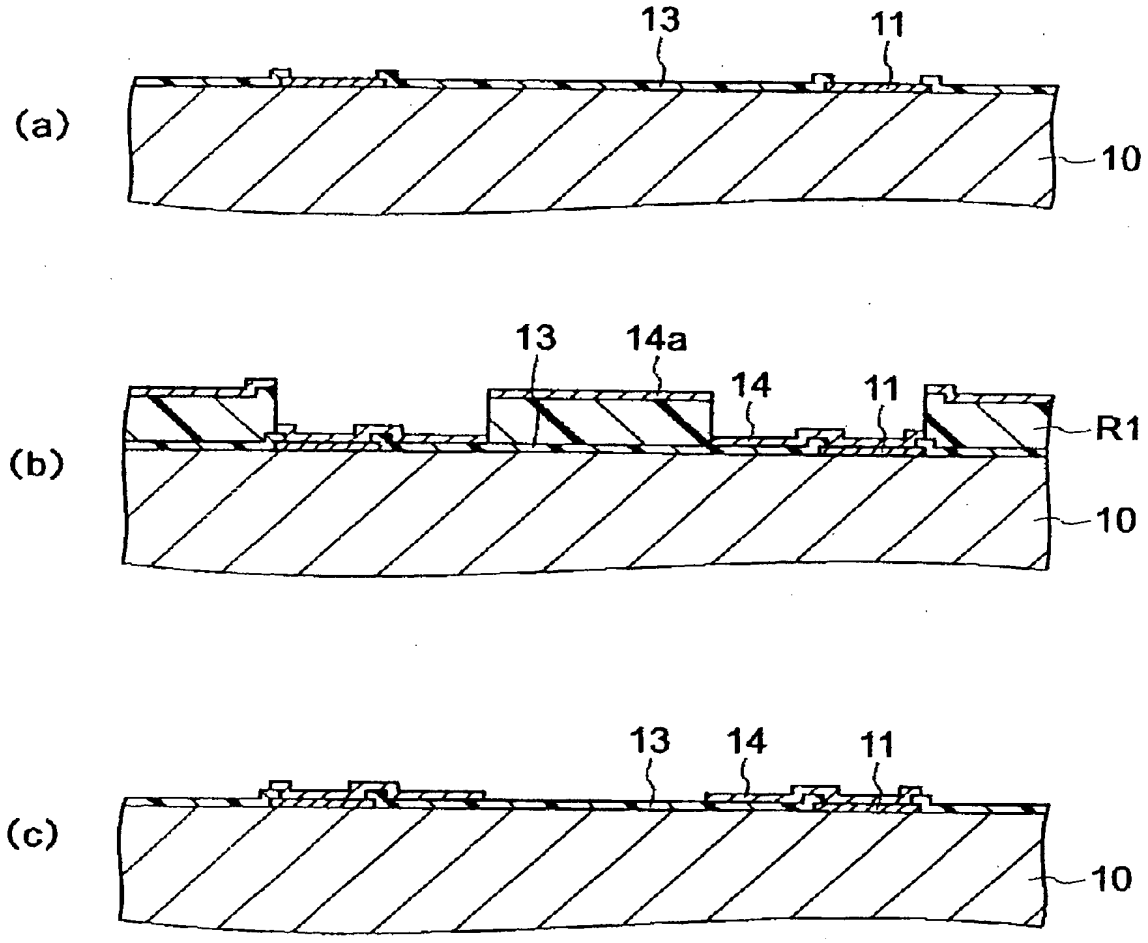
[Description of References]

1...CSP type semiconductor chip; 2... mounting board; 3...sealing resin; 10...semiconductor wafer; 10'...semiconductor chip; 11...electrode pad; 12, 13...surface protective film; 14...conductive film (BLM film); 15...upper surface protective film; 16, 16a... solder layer; 16b...bump; 17...resin film; 17a...insulating impurities; 18, 19...eutectic solder layer; 20...board; 21...lands; 22...precoated solder layer; 23...solder resist; 30...wafer stage; 31...semiconductor wafer; 32...gas ejection nozzle; 34...gas; 35...suction nozzle; 36...reaction treatment chamber; 37...wafer cassette; 38...gate valve; 39...load-lock chamber; 40...gas introduction port; 41...gas exhaust port.

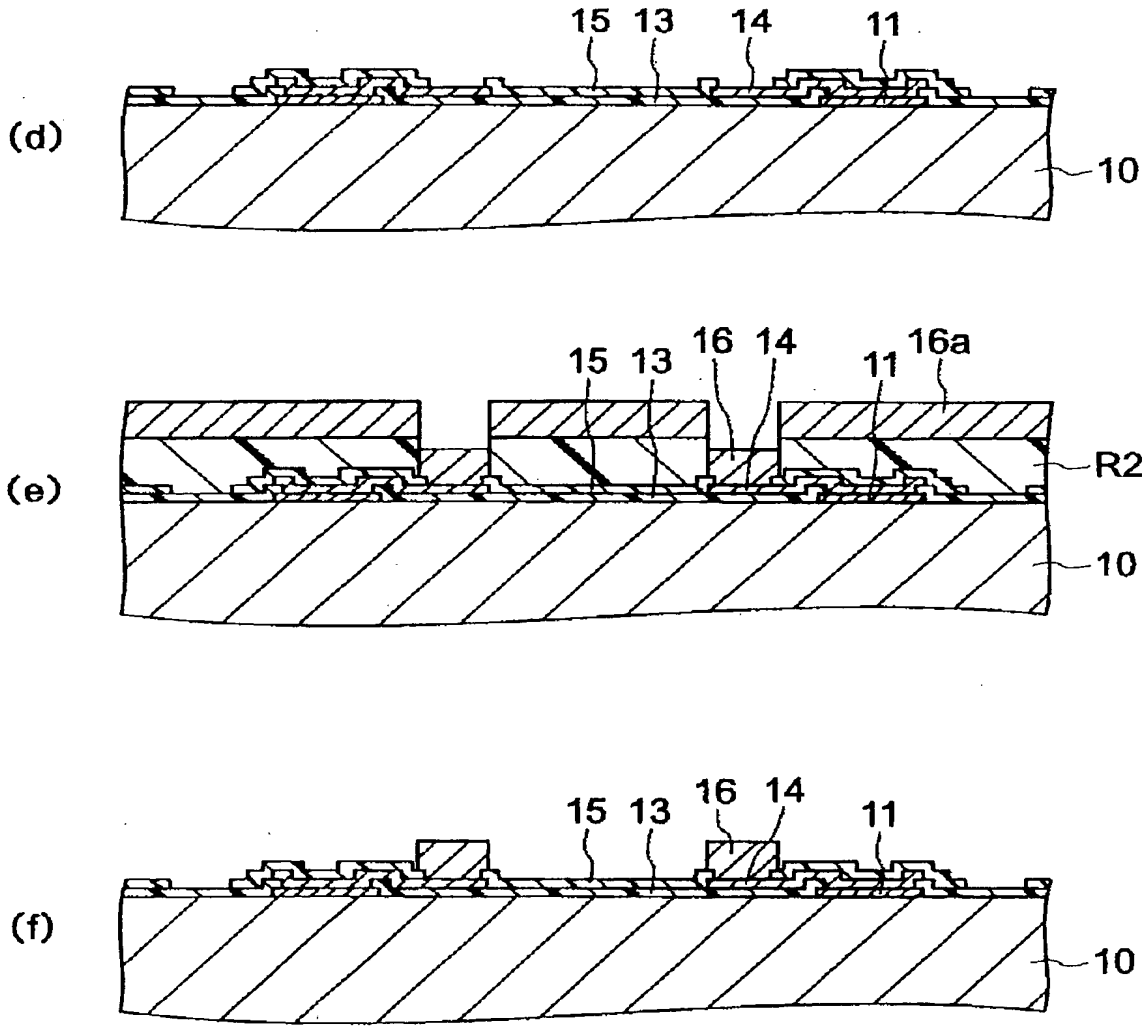
(Name of Documents) Drawings
(FIG. 1)



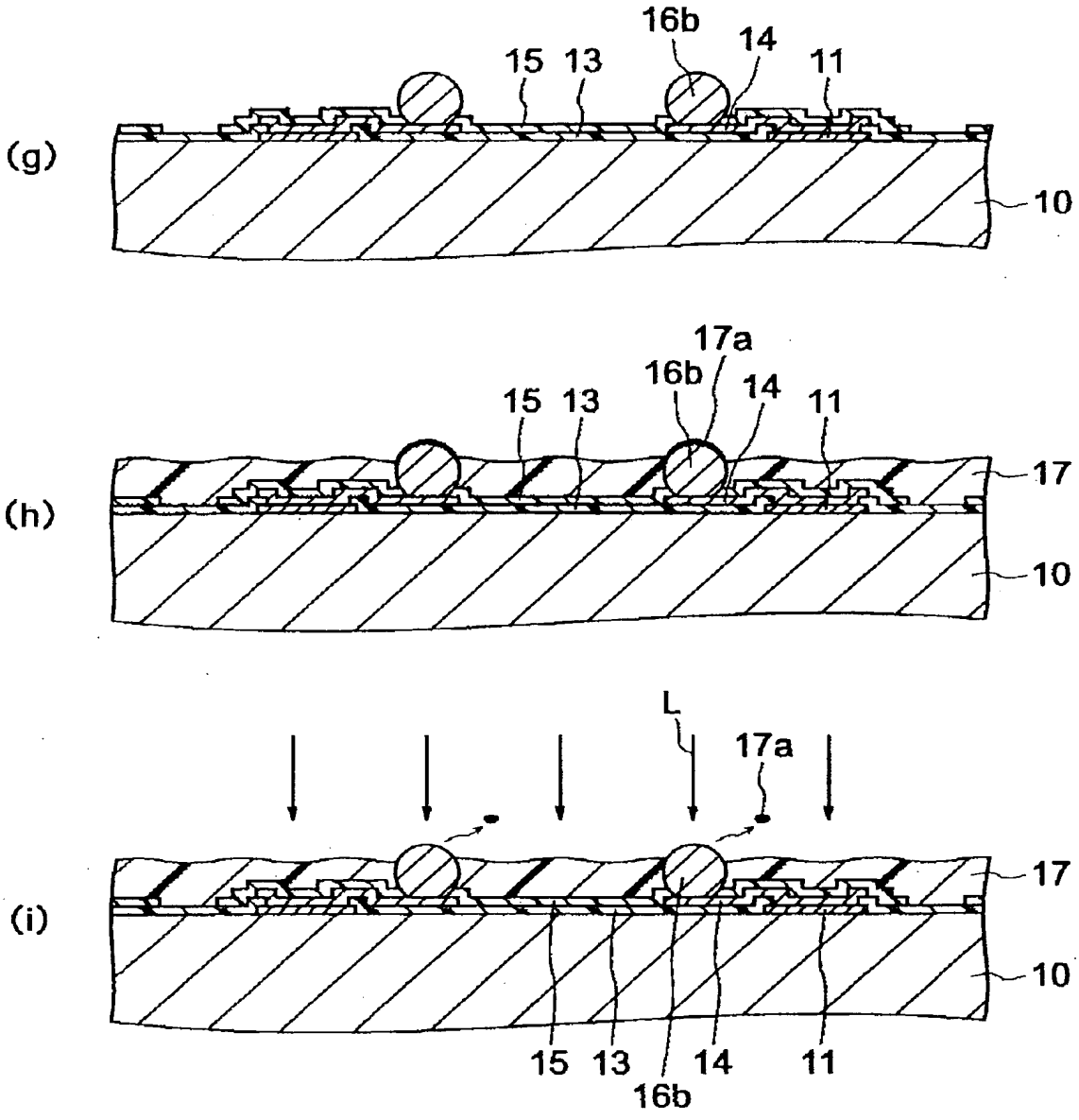
(FIG.2)



(FIG. 3)



(FIG. 4)


(g)
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(h)
17a
16b
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(i)
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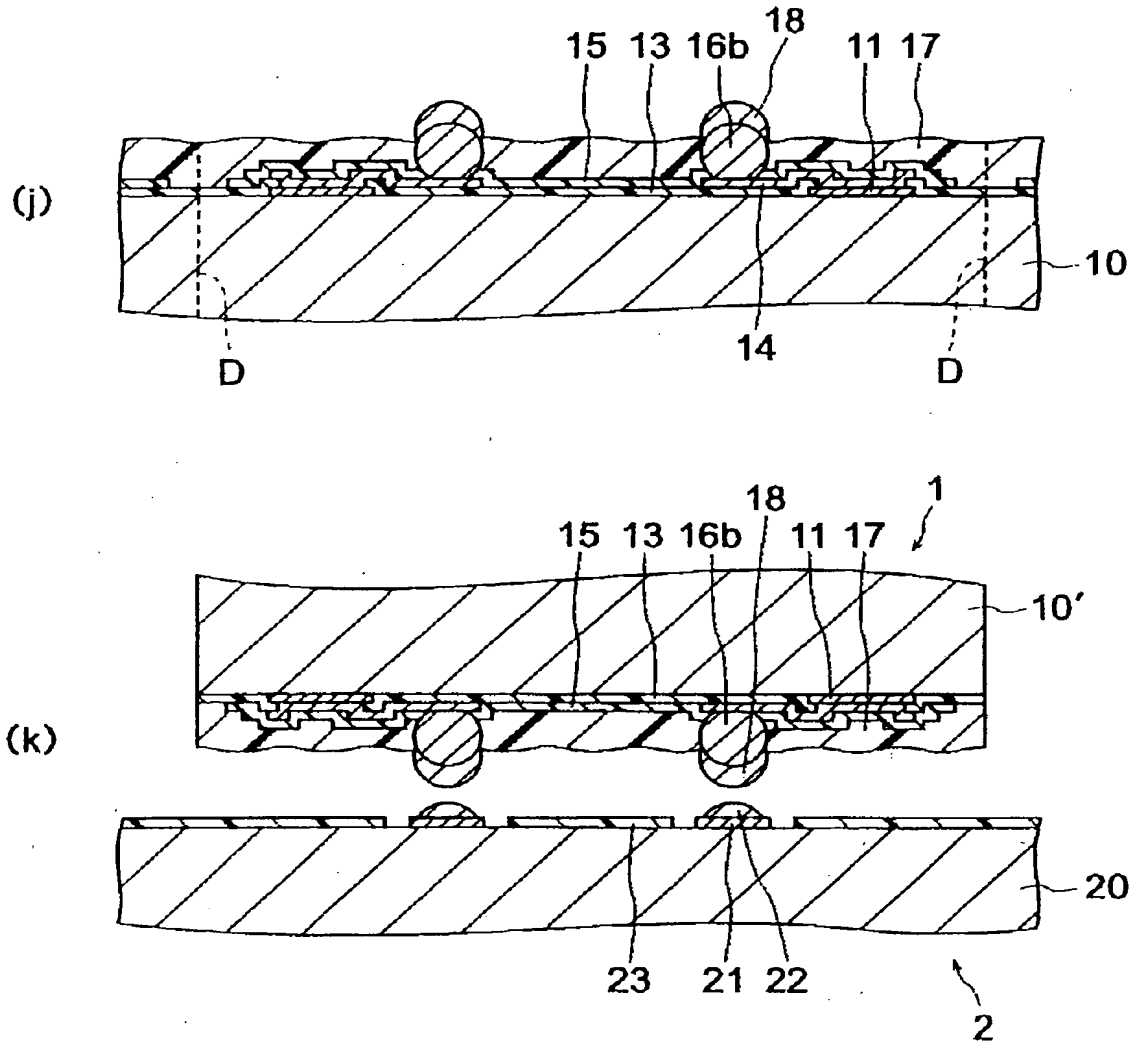
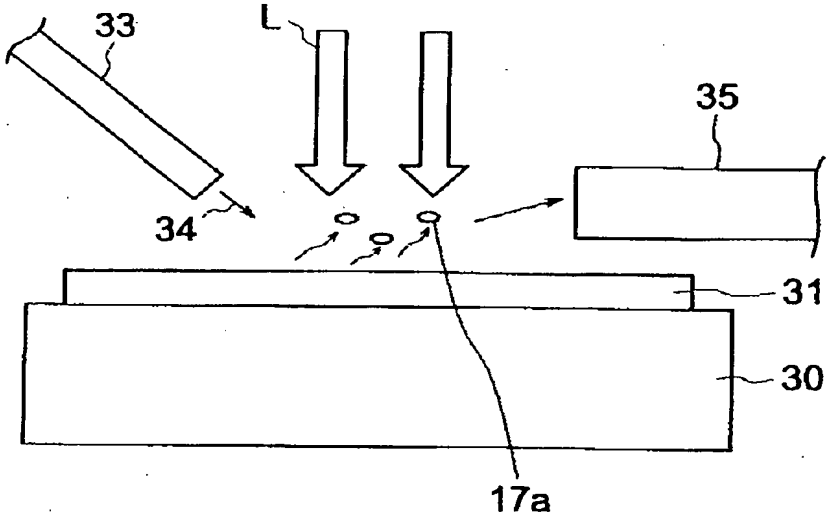
11
16b

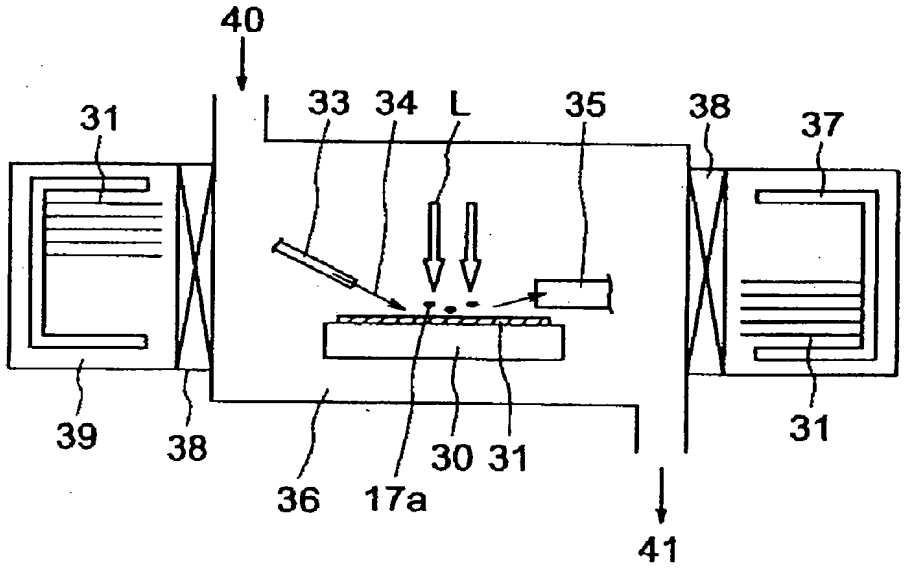
(FIG. 5)



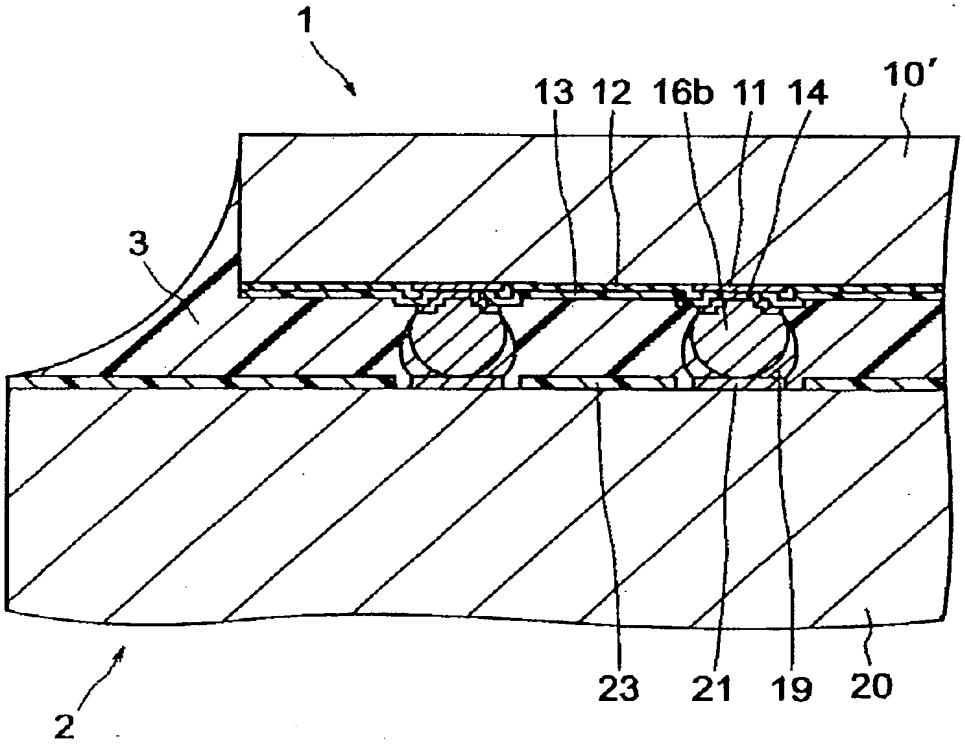
(FIG. 6)



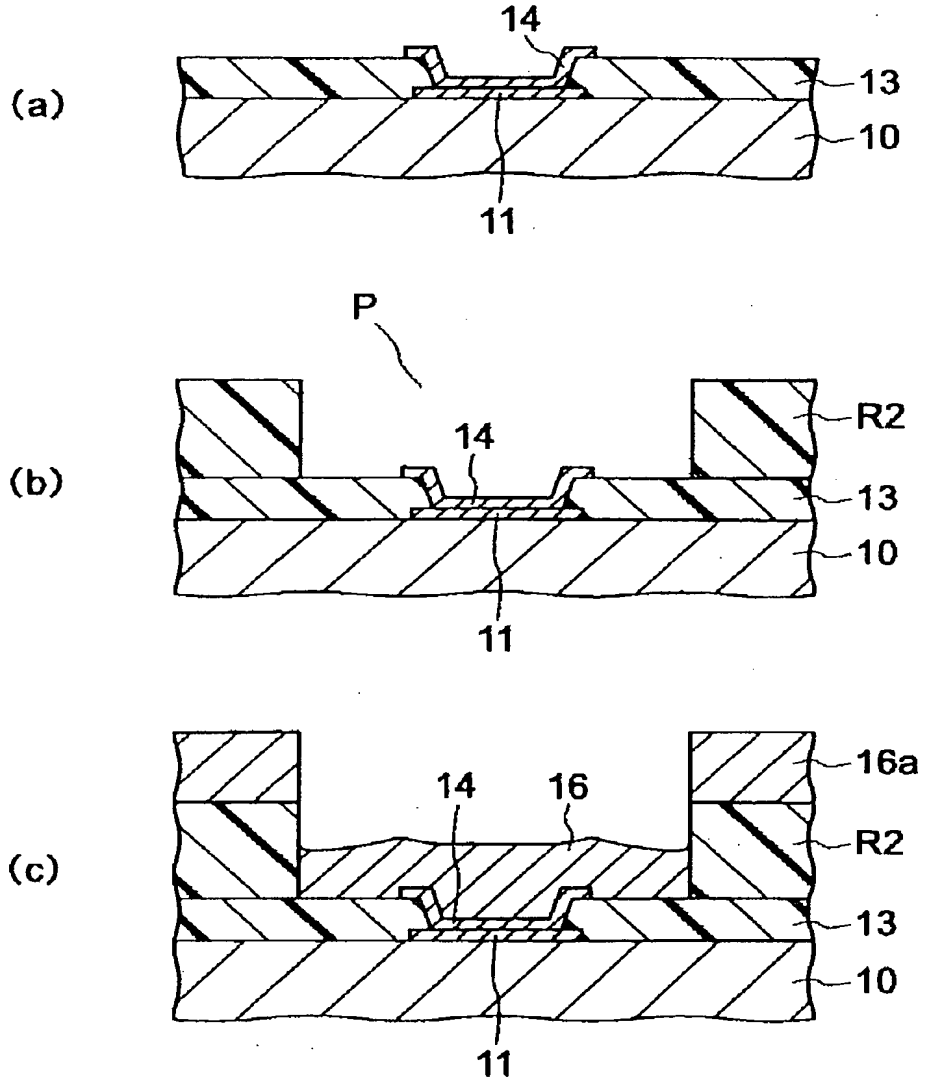
(FIG. 7)



(FIG. 8)

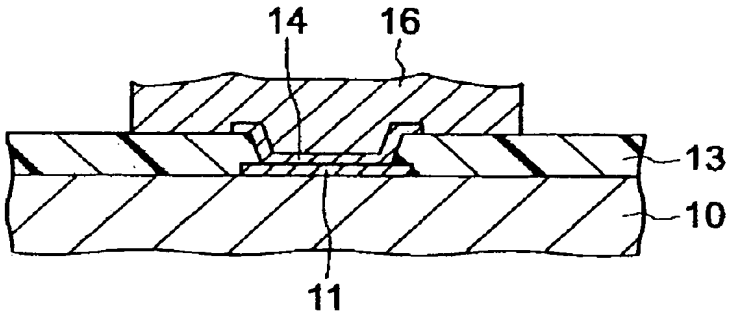


(FIG. 9)

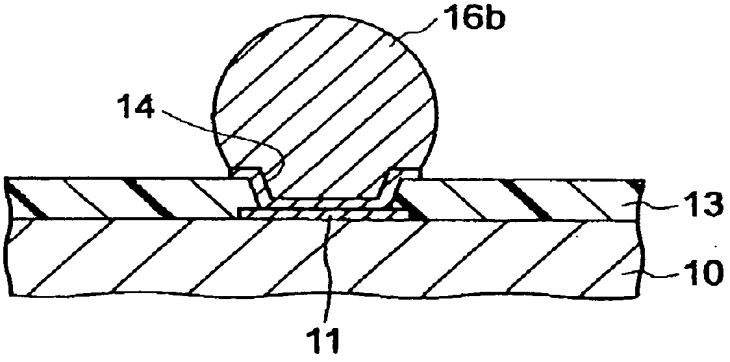


(FIG. 10)

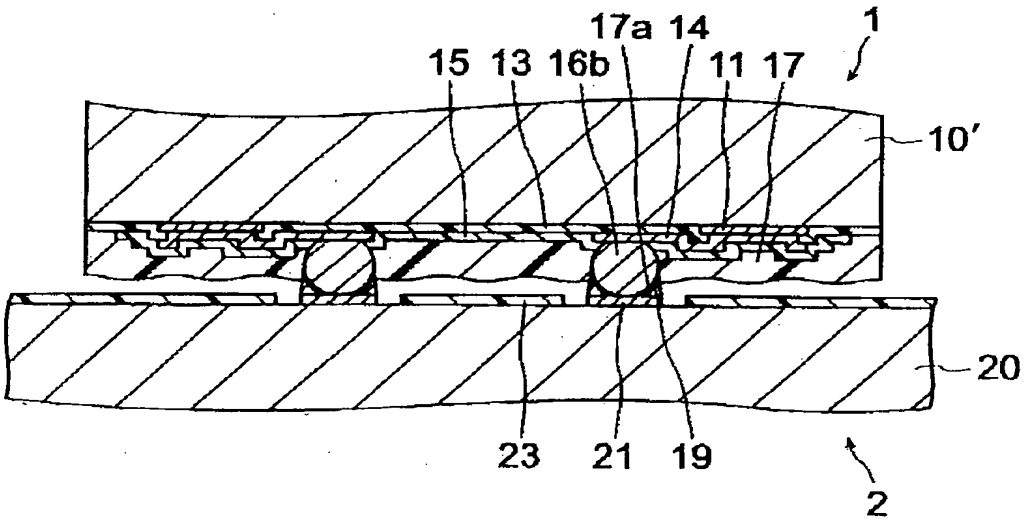
(d)



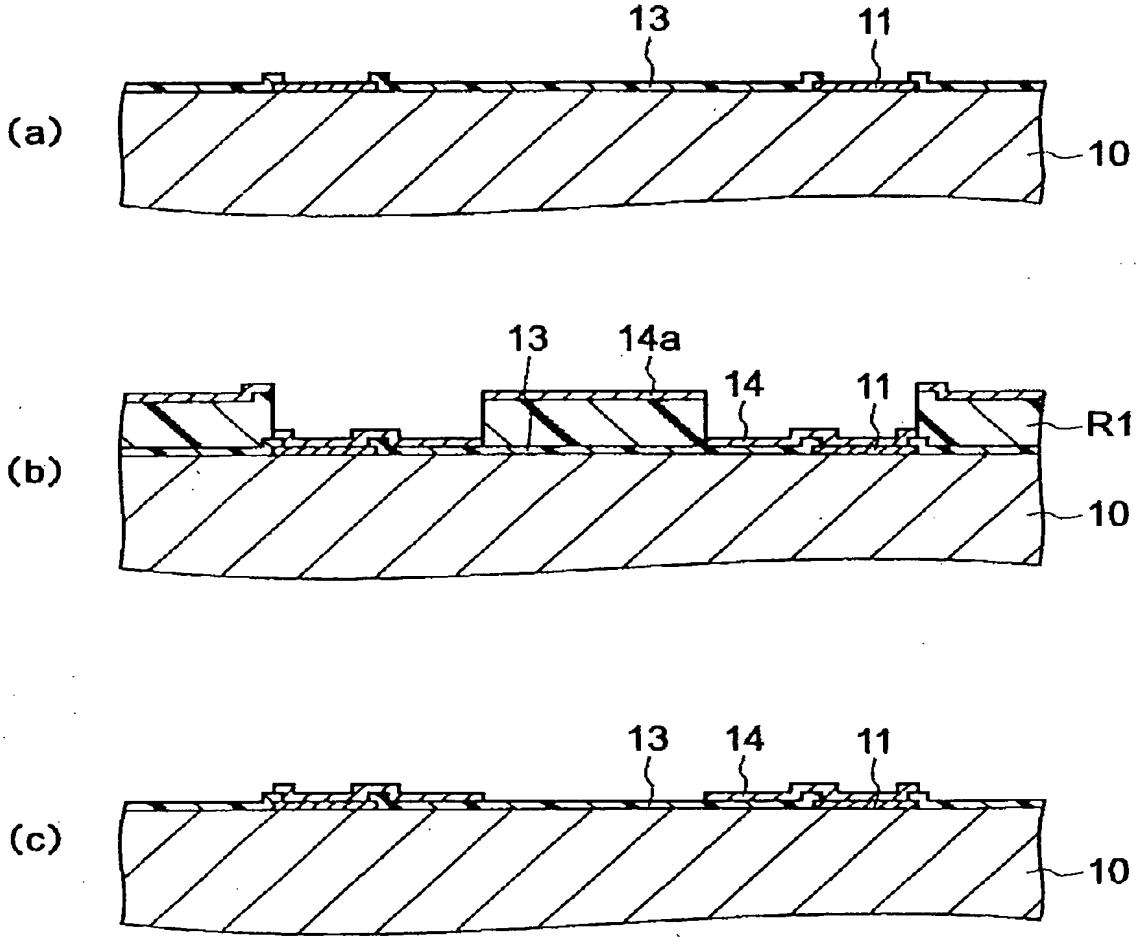
(e)



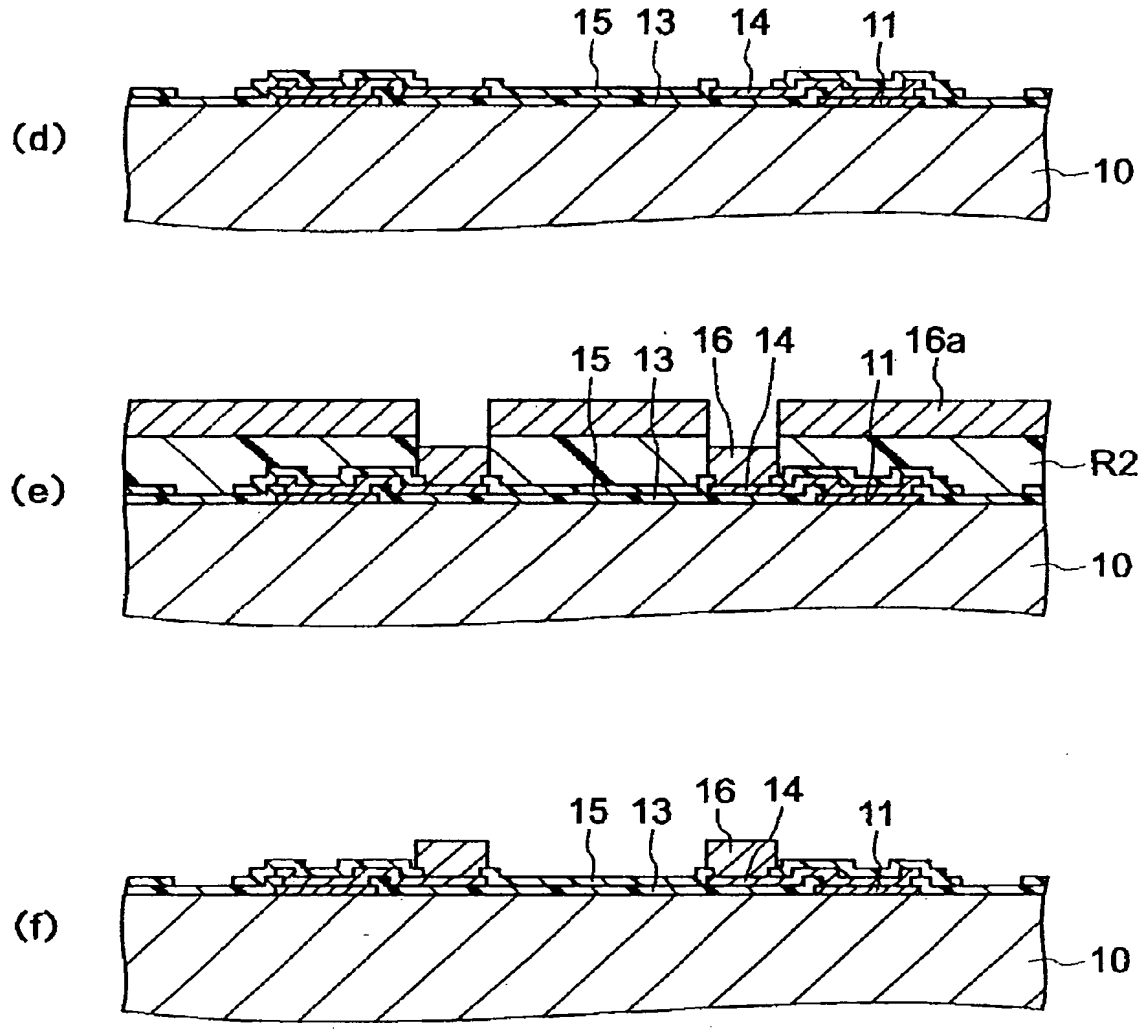
(FIG. 11)



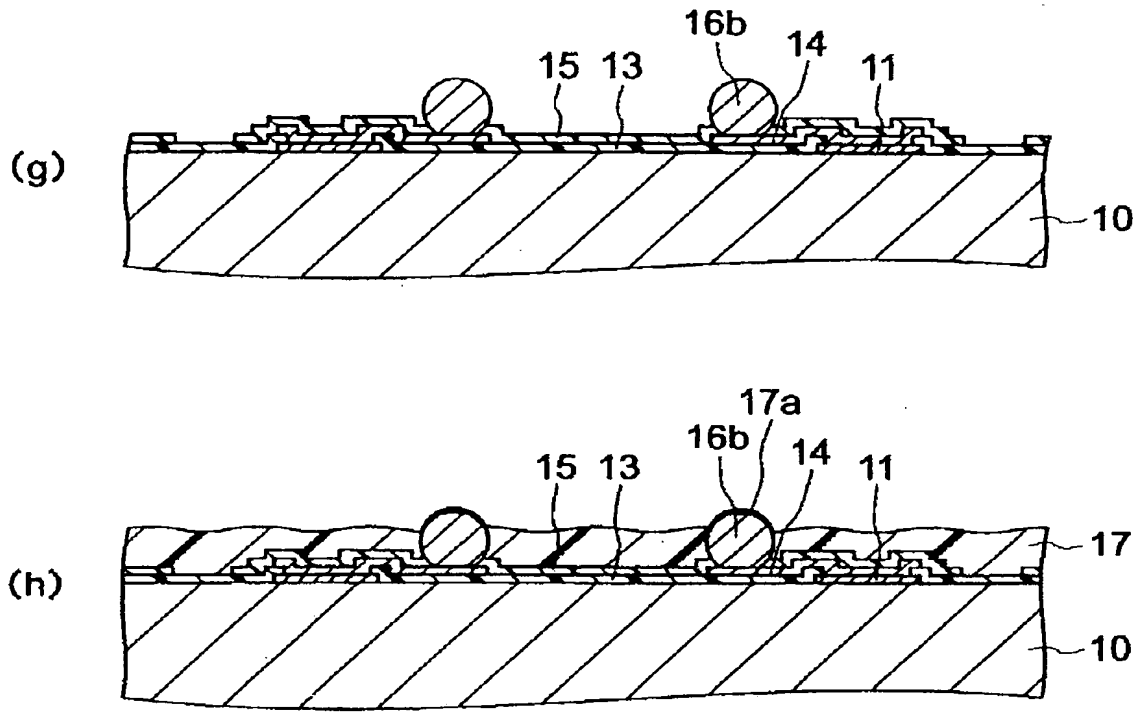
(FIG. 12)



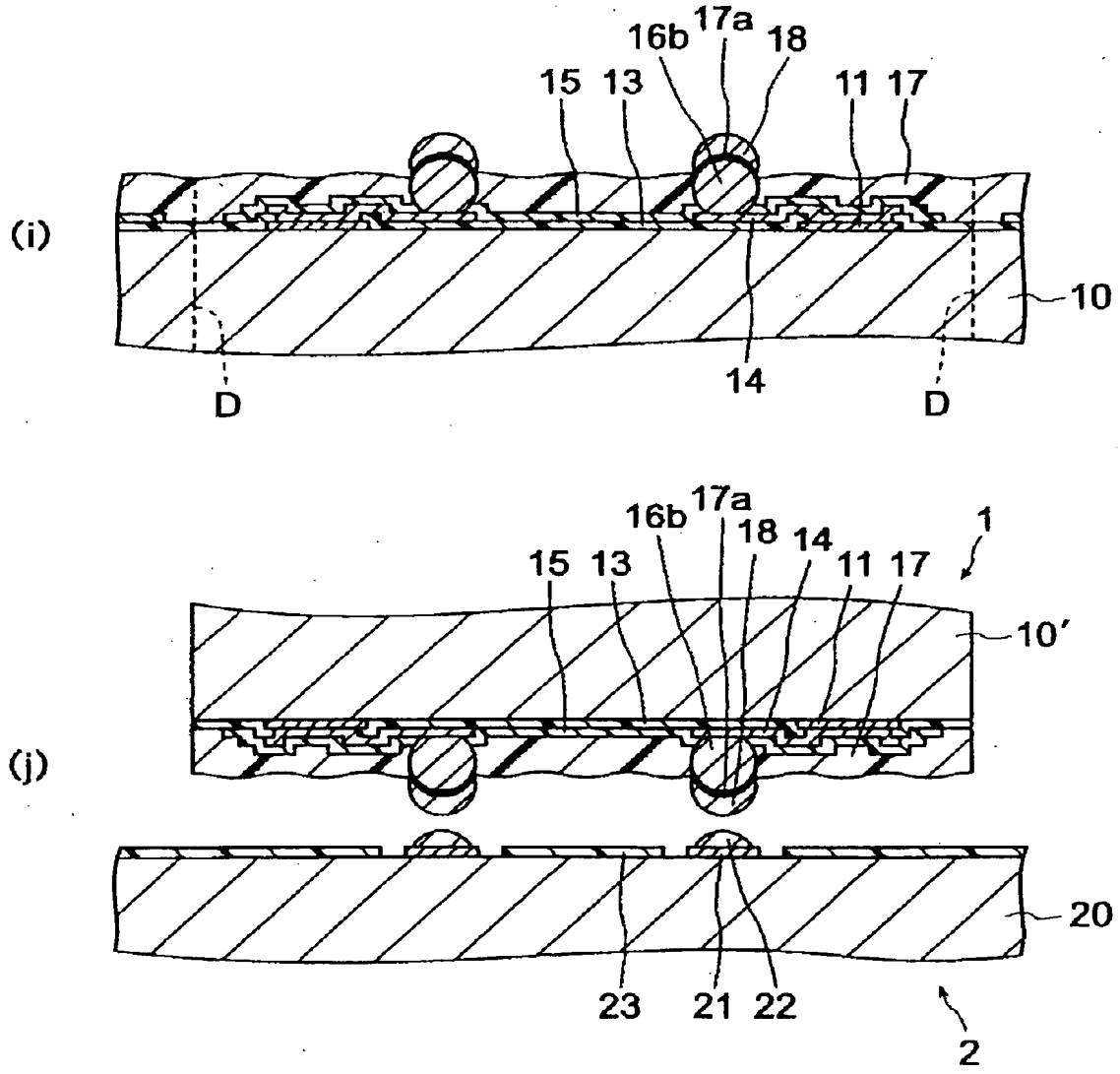
(FIG. 13)



(FIG. 14)



(FIG. 15)


(i)
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(j)
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[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PROBLEM] To provide a method of producing a semiconductor apparatus which can suppress a rise in the electrical resistance and a decline in the joint strength at the bump connection interfaces and improve the connection reliability when using the method of reinforcing the bases of the bumps by a resin film.

[MEANS FOR SOLUTION] A Bumps 16a are formed on a semiconductor wafer 10 formed with pattern circuits of semiconductor chips so as to connect to the circuit pattern, a resin film 17 is formed on the bump forming surface of the semiconductor wafer to a thickness giving a surface lower than the height of the bumps while sealing the spaces between the bumps, an irradiation of laser beam L etc., is applied to cause extremely sharp thermal expansion at a surface portion of the bumps or the energy of the laser beam is applied to reduce the surface portion of the bumps to remove the sealing resin components deposited on the surface of the bumps 16b or natural oxides or other insulating impurities 17a to thereby clean and activate the surfaces of the bumps 16b, and the chip is mounted on a mounting board.

[SELECTED DRAWING] FIG. 4